AN EBS MONITOR THAT THINKS FOR ITSELF

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FCC regulations require each broadcast station to have a monitor which will respond when a monitored station transmits an Emergency Broadcast System (EBS) alert. Complying with the regulation is relatively simple, since all that is needed is a receiver with an AGC system and an alarm which will indicate when the AGC voltage changes (1). The ordinary type of monitor is limited in usefulness, however, because it will respond to any carrier outage, causing considerable operator inconvenience, especially if the monitored station is having transmitter trouble.

There are two cases in which a more accurate monitor is necessary: if the notification is to be logged automatically, or if it is impractical to monitor the audio output frequently. In a facility where a fast-paced show is in progress, and the engineer is in the same studio as the talent, there may be no time to plug headphones into a monitor jack before the alert broadcast is terminated. For these reasons, it is desirable to have an EBS monitor which will be as free as possible from false indications.

To distinguish a false alarm (a carrier drop-out) from a true alarm (carrier off five seconds, on five seconds, off five seconds, 1-kHz tone five seconds), some type of timing and logic is necessary. For maximum reliability, the unit to be described was built with all silicon semiconductors. The logic uses integrated circuits for simplicity and low cost, as well as enhanced reliability. The use of IC's is somewhat novel in broadcast equipment. It will be assumed that the reader has a basic familiarity with the NOR gates and JK flip-flops (2).

Circuit Description

There are two inputs to the monitor: an AGC input and an audio input. The audio input level is not critical, because the signal is clipped to present a constant-amplitude signal to the active filter. Any input greater than —10 dBm should be satisfactory; input impedence is about 600 ohms. This unit was designed to work with a negative AGC voltage which becomes more negative as signal strength increases. The type of IC used requires two voltage levels, 0-0.2 volt, which corresponds to a 0 logic level, and 0.7-3.5 volts, which corresponds to a 1 logic level. It is necessary to translate the audio and AGC voltages to these levels. The AGC voltage is translated to a voltage 6 volts less negative by the input zener diode. The resulting voltage is applied to the input of emitter follower TR3, which raises the input impedance to about 500,000 ohms. The voltage at the emitter is applied to one end of an adjusting potentiometer, the wiper of which goes to the logic-gate input. With the pot set properly, an AGC voltage change of 0.5 volt is sufficient to make the output of G4 change state. With carrier on, the output is high (logic 1), and this causes TR4 to conduct and light I1, indicating presence of carrier.

Translation of the audio is performed by a clipper, active filter, and rectifier so that signals in the range of 900-1100 Hz will give a high logic state. It would be possible to narrow this range considerably, but allowance must be made for inaccurately calibrated oscillators and tape-speed variation at the transmitting station. Clipping is performed by G3, which is biased as an amplifier, and which normally is overdriven considerably by the receive output.

The constant-amplitude output is lowered by R1, which is adjusted to give logic-1 output over the proper bandwidth. The active filter consists of an amplifier whose output is 180° out of phase with its input, and a feedback loop with nonlinear frequency characteristics. The attenuation of network C1-C2-R3-R4 is greatest at 1 kHz. Since this network introduces negative feedback, the amplifier gain increases at 1 kHz. Diode D1 rectifies the filter output to provide DC for the logic circuit.

After the signals from the receiver are converted into logic levels, it is necessary to convert the sequence of these logic signals into ultimate alarm activation. This is done with appropriate timing circuitry and a digital circuit known as a "shift register." The shift register consists of four flip-flops, FF1-FF4. They are so interconnected that no FF can flip until the

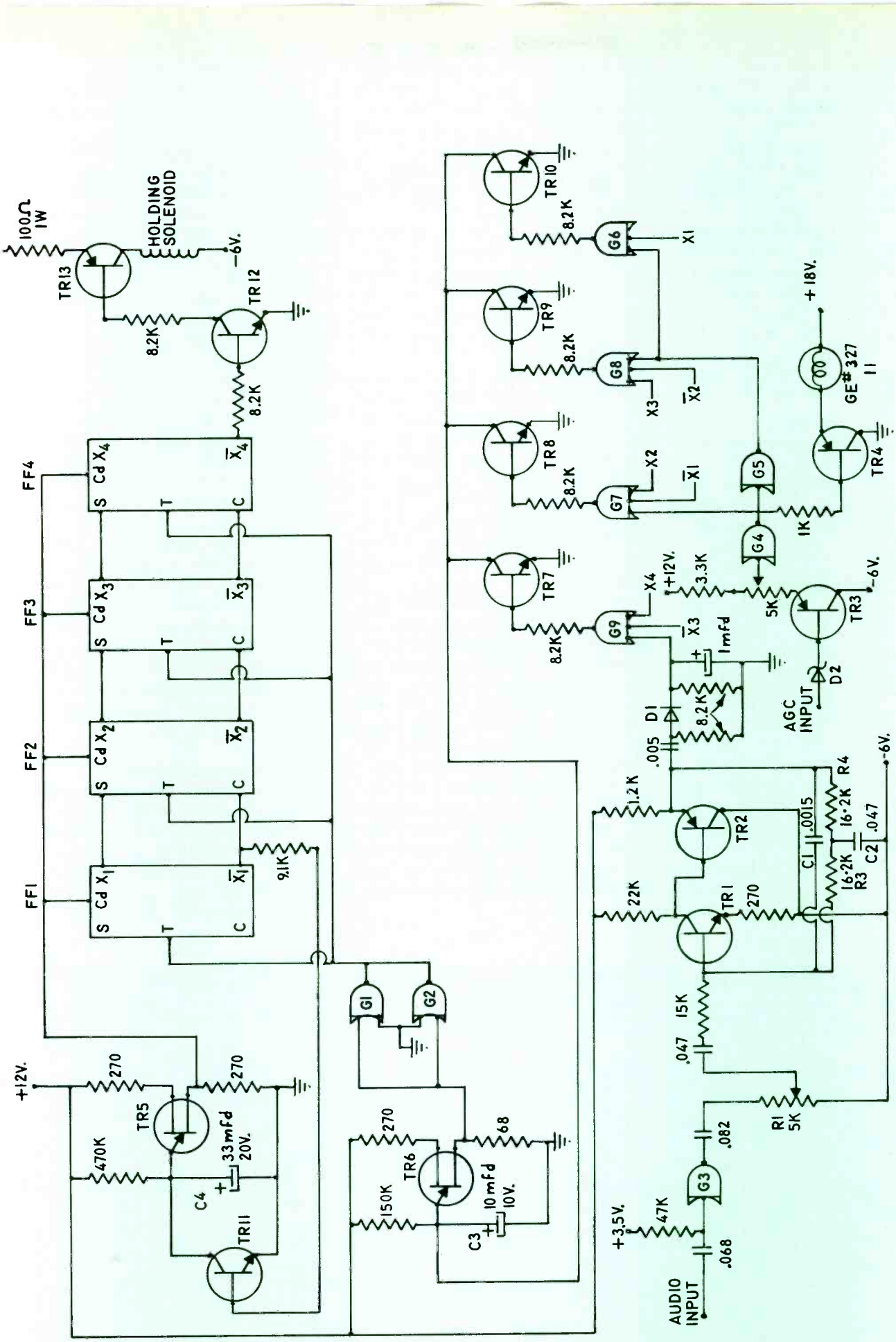
100Ω 1W
HOLDING SOLENOID
-6V.
TR13
TR12
8.2K
8.2K
FF4
FF3
FF2
FF1
S Cd X4 T C X̄4
S Cd X3 T C X̄3
S Cd X2 T C X̄2
S Cd X1 T C X̄1
9.1K
+12V.
270
270
TR5
470K
33 mfd 20V.
C4
TR11
G1
G2
270
68
TR6
150K
10 mfd 10V.
C3
TR10
TR9
TR8
TR7
8.2K
G6
G8
G7
G9
X1
X3
X̄2
X2
X̄1
X4
X̄3
+18V.
GE #327
TR4
G5
G4
1K
+12V.
3.3K
5K
-6V.
TR3
1mfd
D2
AGC INPUT
D1
.005
8.2K
1.2K
TR2
TR1
22K
270
C1 .0015
16·2K R4
16·2K R3
C2 .047
-6V.
.047
15K
R1 5K
.082
G3
+3.5V.
47K
.068
AUDIO INPUT

Fig. 1

one preceeding it has done so. All the flip-flops are triggered simultaneously, but only one can flip on each pulse. Gates G1 and G2 are connected in parallel to comply with the IC loading rules, which specify that a gate cannot trigger more than three flip-flops simultaneously. The trigger pulses come from TR6, a unijunction transistor in a relaxation-oscillator configuration. This stage is timed so that, if left to itself, it will produce a positive pulse every 1.5 seconds or so. Gates G1 and G2 invert the pulse and shorten it to the 100 nanoseconds required by the flip-flops.

After TR6 has produced one pulse, FF1 changes state, and Q1 assumes the low state. Consequently, TR11 stops conducting and enables C4 to charge with a time constant of about 20 seconds. After this time, TR5 produces a positive pulse which resets all the flip-flops. Note that the reset input does not require an extremely fast pulse.

Transistors TR7-TR10 are connected in parallel across C3. Thus, if any of these transistors conducts, no pulse will be generated to trigger the flip-flops.

The logic gates are so arranged that only one transistor at a time is conducting, for example, until there is a break in the carrier, the inputs to G6 are both logic 0, the G6 output is logic 1, and TR10 conducts. When the carrier is interrupted, G5 applies a logic-1 input to G6, the G6 output goes to logic 0, TR10 stops conducting, and C3 begins to charge. After TR6 generates the first timing pulse, output Q1 goes to logic 0; output Q2 is already logic 0, and the output of G4 is logic 0 because there is no carrier.

The output of G7 is therefore logic 1, and TR8 conducts. Capacitor C3 begins charging again when the carrier reappears and the output of G4 becomes logic 1. The next pulse from TR6 causes FF2 to change state.

By a little study, it can be seen that a logic-1 output (logic 0 at the Q outputs) advances through the shift register only when events occur in the specified order and within the specified time (before TR5 resets the flip-flops). When a logic-0 output appears at Q4, TR12 and TR13 stop conducting, and the holding solenoid is released to activate the alarm.

It was stated previously that TR6 will generate a pulse every 1.5 seconds if not subjected to external influences. A 1.5-second timing interval might appear too short, and indeed it is. However, Q7-Q10 will discharge C3 well below the point to which unijunction transistor will discharge it. Thus, the timing interval is increased to about 2.5-3 seconds. Since most EBS transmissions are sent manually, it is desirable to leave some margin of error for the transmitter operator. If less margin is desired, add a few microfarads to C3.

External Connection

So far, little has been said about the actual connection of the alarm unit. There is an excellent article in the January 1968 issue of **Broadcast Engineering** (1) covering both receiver connection and different relay arrangements. The relay arrangement to be used will depend on requirements of your station.

It is particularly difficult to derive AGC voltage from your receiver, you may wish to use an integrated circuit known as a voltage comparator. This circuit compares two input signals and changes logic level when one signal is only a few millivolts from a preset reference. Fig. 2 shows a sample hookup of this circuit. Be sure to obtain the manufacturer's data and application notes for the unit you plan to use.

The power supply (Fig. 3) for the original unit must supply several voltages: —6, 0, 3.5, 12, and 18 volts. It should be possible to design the alarm unit to use fewer voltages. In fact, if a 12-volt solenoid-held switch and 12-volt pilot lights were used, only the 12- and 3.5-volt sources would be necessary.

Special Components

The integrated logic circuits used here are members of the Motorola MC700P series. It will be noticed that several inputs to the dual gates are not used, and two complete gates are not used. All the unused inputs should be grounded. (It

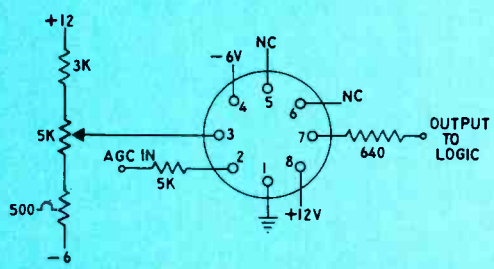

Fig. 2

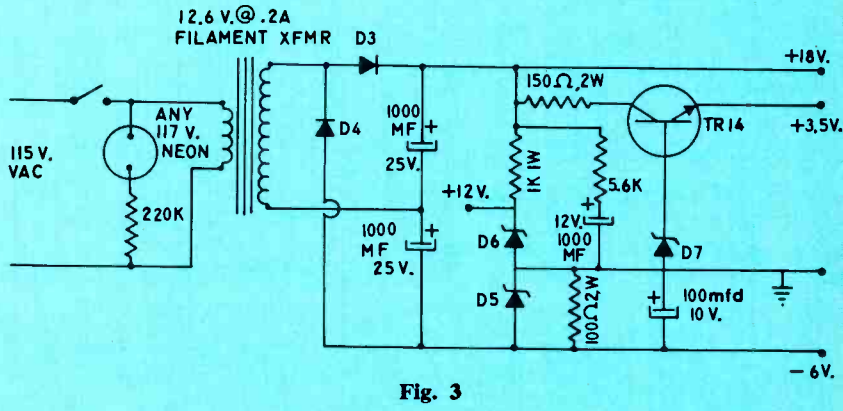

Fig. 3

would be possible to save a few pennies by purchasing the precise number of gates required.) Fig. 4 shows the pin connections of the IC's used; don't forget to connect the ground and the 3.5 volts to each IC, even though these connections are not shown on the schematic.

A combination reset switch and holding solenoid is used in this EBS monitor. Such devices are manufactured by Microswitch and other companies. If there is a voltage on the holding solenoid, the switch remains in when pressed. (The solenoid will not pull in the switch, however.) Thus, if the solenoid is released, the switch will pop out and open (or close) the contacts. It will remain in this position until reset. If the switch is connected to the alarm, lights, etc., the one unit performs two functions. Of course, it is always possible to use a switch and a relay.

Conclusion

This EBS monitor has many advantages over the usual type. If you are troubled by false alarms, or don't have time to investigate every time the warning comes on, the added complexity of this unit is well worth the effort. Even if you don't need it desperately, it is relatively inexpensive and will provide valuable experience in working with IC's. ▲

References

1. Building EBS Receivers, Charles D. Sears, **Broadcast Engineering,** 1968, p 20.
2. Digital Circuits for Broadcasters, J. L. Smith, **Broadcast Engineering,** February 1968, p 12; March 1968, p 29; April 1968, p 24; and June 1968, p 26.

Parts List

TR, 7, 8, 9, 10, 11, 12, 2N4074
TR3, 13 2N3638
TR4 2N3053
TR5, 6 2N2646
TR14 2N3053

Any of these transistors can be substituted for types with even remotely similar characteristics.

FF1-FF4 MC790P
G7-G9 each ⅓ MC792P
G1-G6 each ¼ MC724P
D1, D3, D4 IN3193
D2 1N754
D5 1N3016
D6 1N4742
D7 1N3823

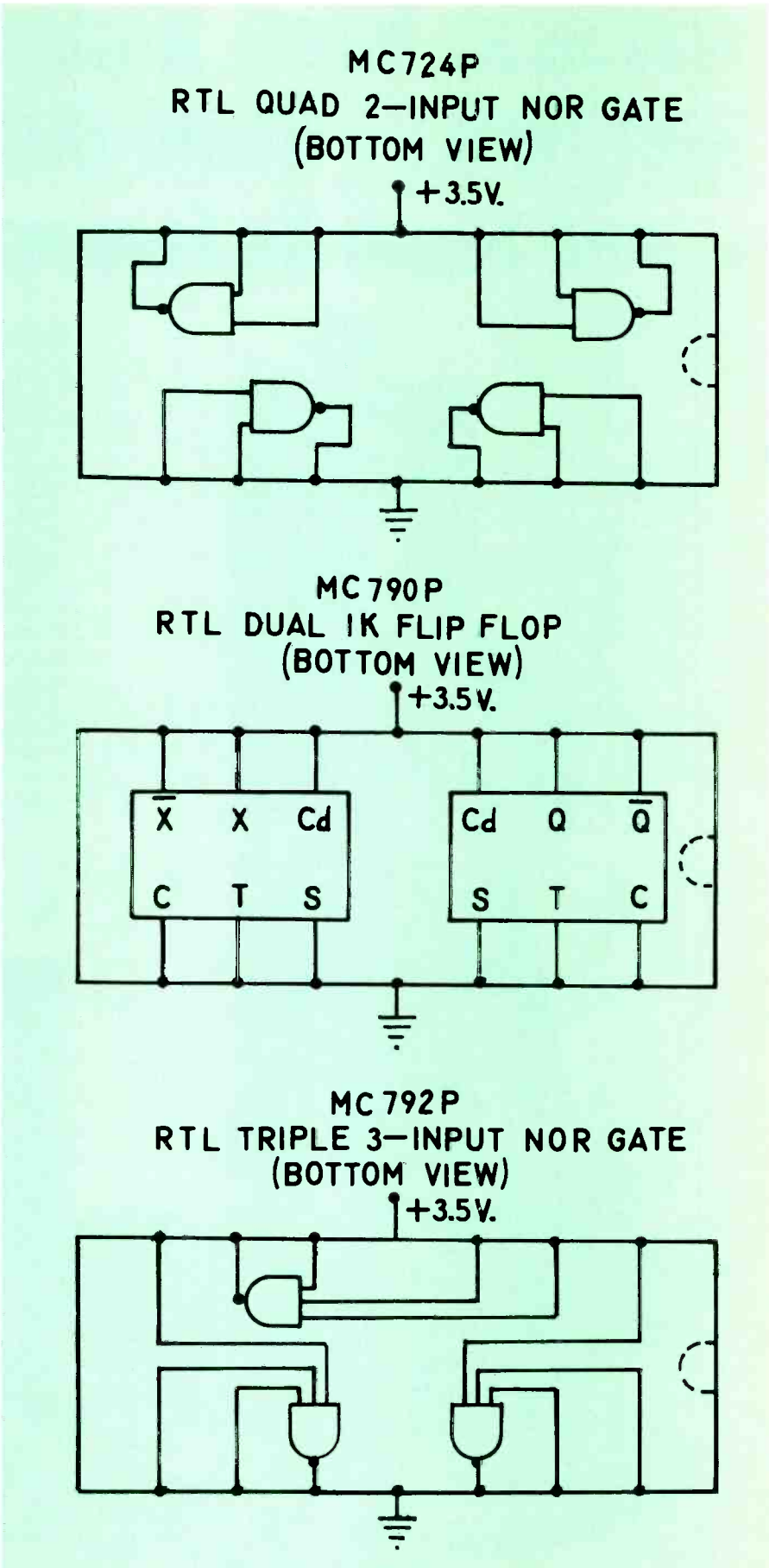

Fig. 4